IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket Number 17403US05

In re Application of MacInnis	)	
	)	
Serial No.: 10/763,087	)	**Electronically Filed**
	)	
Filing Date: 9/15/2010	)	**August 18, 2011**
	)	
Examiner: Hassan	)	
	)	
Confirmation No.: 6408	)	
	)	
Art Unit No. 2182	)	

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This amendment is filed in response to the Final Office Action mailed 9/15/2010. On 1/18/2011, Appellant filed a Notice of Appeal, a Pre-appeal Request for Conference, and Pre-Appeal Brief. On August 1, 2011, Appellants were advised to proceed to the Board of Patent Appeals and Interferences.

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I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 5300 California Drive, Irvine California 92617, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefore.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 4, 5, 7-10, and 12 are presently pending.

Claims 4, 5, 7-10, and 12 are rejected under 35 U.S.C. 103(a) as obvious from the combination of U.S. Patent 5,949,439 (Ben-Yoseph), in view of U.S. Patent 6,351,474 (Robinett), and further in view of U.S. Patent 6,070,231 (Ottinger).

IV. STATUS OF AMENDMENTS

There are no amendments pending in this application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A unified memory system (page 7, Lines 4-5) comprising:

a memory that is shared by a plurality of devices including at least a central processing unit and a graphics processing unit (page 7, Lines 7-10);

a memory request arbiter coupled to the memory, wherein the memory request arbiter performs real time scheduling of memory requests from different devices having different priorities, the unified memory system provides for real time scheduling of tasks, and provides access to memory by requesters that are sensitive to latency and do not have determinable periodic behavior (p. 120, lines 9-17);

dual memory controllers, the dual memory controllers including a first memory controller and a second memory controller (p. 120, Lines 19-29), the memory request arbiter including a first arbiter coupled to the first memory controller and a second arbiter coupled to the second memory controller (p. 121, Lines 4-17), wherein the first arbiter and the second arbiter perform real time scheduling of memory requests, wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter based on the address of the memory request (p. 121, Lines 19-29); and

a memory select circuit receiving requests from the central processing unit and graphics processing unit, selecting one of the dual memory controllers and one of the first arbiter or second arbiter, and providing the request to the selected one of the dual memory controllers and the selected one of the first arbiter or second arbiter (p. 121, Lines 19-29); and

wherein a predetermined minimum interval between subsequent accesses by a device is enforced, and wherein said predetermined minimum interval is long enough for another device to access (p. 124, Line 22 – p. 125, Line 5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 4, 5, 7-10, and 12 are obvious from the combination of U.S. Patent 5,949,439 (Ben-Yoseph), in view of U.S. Patent 6,351,474 (Robinett), and further in view of U.S. Patent 6,070,231 (Ottinger).

VII. ARGUMENT: CLAIMS 4

Claim 4 is copied below:

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4. (Previously Presented) A unified memory system comprising:

a memory that is shared by a plurality of devices including at least a central processing unit and a graphics processing unit;

a memory request arbiter coupled to the memory, wherein the memory request arbiter performs real time scheduling of memory requests from different devices having different priorities, the unified memory system provides for real time scheduling of tasks, and provides access to memory by requesters that are sensitive to latency and do not have determinable periodic behavior;

dual memory controllers, the dual memory controllers including a first memory controller and a second memory controller, the memory request arbiter including a first arbiter coupled to the first memory controller and a second arbiter coupled to the second memory controller, wherein the first arbiter and the second arbiter perform real time scheduling of memory requests, wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter based on the address of the memory request; and

a memory select circuit receiving requests from the central processing unit and graphics

processing unit, selecting one of the dual memory controllers and one of the first arbiter or second arbiter, and providing the request to the selected one of the dual memory controllers and the selected one of the first arbiter or second arbiter; and

wherein a predetermined minimum interval between subsequent accesses by a device is enforced, and wherein said predetermined minimum interval is long enough for another device to access.

The rejection to claim 4 should be REVERSED for any of the following reasons: (1) the combination does not teach "a memory request arbiter;" (2) "a memory request arbiter … provides access to memory by requesters that are sensitive to latency and do not have determinable periodic behavior"; (3) "a predetermined minimum interval between subsequent accesses by a device is enforced, and wherein said predetermined minimum interval is long enough for another device to access"; and (4) wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter based on the address of the memory request.

A. ARGUMENT: THE COMBINATION DOES NOT TEACH "A MEMORY REQUEST ARBITER;"

The Final Office Action indicates that Ben-Yoseph teaches "a memory request arbiter coupled to the memory (resource manager 308)." Final Office Action at 2.

Appellants respectfully submit that the foregoing is in error. Although "resource manager 308 manages the Rambus DRAM memory 110, maintains execution priorities, and configures block and direct-communication transfers", the resource manager 308 is not an arbiter.

Rather, the resource manager 308 is more akin to a manager that manages multi-tasking, including prioritizing different tasks. However, Ben-Yoseph does not teach that the resource manager 308 specifically resolves memory access contentions.

Accordingly, for at least the foregoing reason, Assignee respectfully submits that the rejection to claim 4 should be REVERSED.

B. ARGUMENT: THE COMBINATION DOES NOT "A MEMORY REQUEST ARBITER … PROVIDES ACCESS TO MEMORY BY REQUESTERS THAT ARE SENSITIVE TO LATENCY AND DO NOT HAVE DETERMINABLE PERIODIC BEHAVIOR"

The Office Action indicates that Ben-Yoseph teaches "access to memory by requesters that are sensitive to latency and do not have determinable periodic behavior (Col. 8, lines 22-36)."

Assignee respectfully submits that the foregoing finding is in error. Latency is defined in the computer context as "the time required to locate the first bit or character in a storage location, expressed as access time minus word time."
http://dictionary.reference.com/browse/latency

Although Ben-Yoseph discuses a software queue, with read pointers and write pointers, the foregoing does not discuss "access to memory by requesters that are sensitive to latency". While Ben-Yoseph teaches that the processor might be quick to locate the element in the software queue, it does not follow that the particular element in the queue is from a requester that is sensitive to the time require to located the first bit or character in a storage location, expressed as access time.

Accordingly, for at least the foregoing reason, Assignee respectfully submits that the rejection to claim 4 should be REVERSED.

C. CLAIM 1 SHOULD BE REVERSED BECAUSE "A PREDETERMINED MINIMUM INTERVAL BETWEEN SUBSEQUENT ACCESSES BY A DEVICE IS ENFORCED, AND WHEREIN SAID PREDETERMINED MINIMUM INTERVAL IS LONG ENOUGH FOR ANOTHER DEVICE TO ACCESS"

The Office Action indicates that the foregoing is taught at Robinett, column 7, lines 50-67. Robinett is directed to a "Network Distributed Remultiplexer for Video Program Bearing Transport Streams". Robinett teaches assinging a dispatch time to the allocated descriptor of the transmit queue, depending on, for example, a receipt time of the transport packet to which the descriptor points and an internal buffer delay between receipt and output of the transport packet. Each transport packet is outputted in a time slot at a particular dispatch time, corresponding to a predetermined delay in the remultiplexer node. If more than one transport packet is to be outputted in the same time slot, each transport packet is outputted in a separate consecutive time slot.

Assignee respectfully submits that the foregoing finding is in error. It is first noted that Robinett is blind to the device originating the transportation packets. Therefore, not "predetermined minimum interval between subsequent access by ***a*** device is enforced". Robinett merely describes a first come, first serve transmission. Note that if the access time of a device is defined as the time the transport packet is placed in the queue, there is no time restriction against the same device placing another

transport packet in the queue. If the time of access is defined as the time of transmission, there is no restriction against the same device transmitting two consecutive packets. In contrast, Assignee claims "wherein a predetermined minimum interval between *subsequent accesses by a device is enforced*, and wherein said predetermined minimum interval is *long enough for another device to access*".

Accordingly, for at least the foregoing reason, Assignee respectfully submits that the rejection to claim 4 should be REVERSED.

D. THE COMBINATION DOES NOT TEACH "WHEREIN MEMORY REQUESTS TO THE MEMORY SHARED BY THE PLURALITY OF DEVICES *ARE ROUTED TO A PARTICULAR ONE OF THE FIRST ARBITER AND THE SECOND ARBITER BASED ON THE ADDRESS OF THE MEMORY REQUEST*"

The Final Office Action indicates that Ottinger teaches the foregoing at Figure 4. Although Figure 4 shows an arbitration scheme utilized by the first arbiter and the second arbiter, col. 16, lines 10-12, Ottinger does not teach that requests are routed to a particular arbiter based on the address memory request. A review of columns 16-18 of Ottinger shows the description of Figure 4 only discusses the first arbiter and does not even discuss the second arbiter. Presumably, the same algorithm could be used by the second arbiter. However, Figure 4 clearly does not show routing to one or the other based on the address of the memory request.

Accordingly, for at least the foregoing reason, Assignee respectfully submits that the rejection to claim 4 should be REVERSED.

CONCLUSION

For the foregoing reasons, claims 4, 5, 7-10, and 12 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: August 18, 2011

Respectfully submitted,

/Mirut Dalal/

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CLAIMS APPENDIX

CLAIM LISTING

1-3. (Cancelled).

4. (Previously Presented) A unified memory system comprising:

a memory that is shared by a plurality of devices including at least a central processing unit and a graphics processing unit;

a memory request arbiter coupled to the memory, wherein the memory request arbiter performs real time scheduling of memory requests from different devices having different priorities, the unified memory system provides for real time scheduling of tasks, and provides access to memory by requesters that are sensitive to latency and do not have determinable periodic behavior;

dual memory controllers, the dual memory controllers including a first memory controller and a second memory controller, the memory request arbiter including a first arbiter coupled to the first memory controller and a second arbiter coupled to the second memory controller, wherein the first arbiter and the second arbiter perform real time scheduling of memory requests, wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter based on the address of the memory request; and

a memory select circuit receiving requests from the central processing unit and graphics processing unit, selecting one of the dual memory controllers and one of the first arbiter or second arbiter, and providing the request

to the selected one of the dual memory controllers and the selected one of the first arbiter or second arbiter; and

wherein a predetermined minimum interval between subsequent accesses by a device is enforced, and wherein said predetermined minimum interval is long enough for another device to access.

5. (Previously Presented) The unified memory system of claim 4, wherein the central processing unit and the graphics processing unit are sensitive to latency and do not have determinable periodic behavior.

6. (Cancelled)

7. (Previously Presented) The unified memory system of claim 4 further comprising a circuit component associated with one or more devices and coupled between the associated devices and the memory request arbiter, wherein the circuit component is used to enforce at least a predetermined minimum interval between subsequent accesses by the associated device to the memory.

8. (Previously Presented) The unified memory system of claim 7 wherein the devices associated with the circuit component include a CPU.

9. (Previously Presented) The unified memory system of claim 7 wherein the devices associated with the circuit component make high priority service requests to access the memory through the circuit component.

10. (Previously Presented) The unified memory system of claim 7 further comprising a round robin server for handling low priority tasks.

11. (Cancelled)

12. (Previously Presented) The unified memory system of claim 10, wherein the round robin server handles only low priority tasks.

EVIDENCE APPENDIX

There are no pages in this appendix

RELATED PROCEEDINGS APPENDIX

There are no pages in this Appendix.